AF/2774

PATENT
P54766

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS AND INTERFERENCES

In re Application of: **Appeal No.**_____

GEUN-WOO PARK

Serial No.: 08/922,300 Examiner: M. MARC-COLEMAN

Filed: 2 September 1997 Art Unit: 2774

For: DISPLAY DEVICE WITH POWER INTERRUPTION DELAY FUNCTION

TRANSMITTAL OF APPELLANT'S BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

Accompanying this transmittal are Appellant's Brief in triplicate in support of the Notice of Appeal filed on 9 January 2004.

Since the prosecution was re-opened with new ground of rejection, Appellant believes that the fee for filing an Appellant's Brief previously filed on 25 September 2000 applies to the present Appellant's Brief (*see* MPEP § 1208.02).

Should the fee for filing the present Appellant's Brief or other fees be incurred however, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Appellant's undersigned attorney in the amount of such fees.

Respectfully submitted,

Robert E. Bushnell
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Folio: P54766
Date: 9 March 2004
I.D.: REB/kf

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Geun-Woo PARK

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ATTENTION: Board of Patent Appeals and Interferences

APPELLANT'S BRIEF (37 CFR §1.192)

This brief is in furtherance of the Notice of Appeal filed in this case on 9 January 2004.

The fees required under §1.17(f) for the filing of the Appellant's Brief are dealt with in the accompanying transmittal letter.

This brief is transmitted in triplicate (37 CFR §1.192(a)).

REPLY BRIEF

I. STATEMENT OF REAL PARTY IN INTEREST

Pursuant to 37 CFR §1.192(c)(1) the real party in interest is:

SamSung Electronics Co., Ltd.
416 Maetan-dong, Yeongtong-gu,
Suwon-si, Gyeonggi-do,
Republic of Korea

II. RELATED APPEALS AND INTERFERENCES

Pursuant to 37 CFR §1.192(c)(2), there are no appeals nor interferences known to the Appellant, the Appellant's legal representative, or the Assignee (real party of interest) which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-11 have been finally rejected and are appealed herein.

IV. STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendment has been filed after receipt of the final rejection (Paper No. 29).

V. SUMMARY OF THE INVENTION

Page 10, line 5 - Page 13, line 11

Fig. 3 is a detailed circuit diagram illustrating the construction of a display device with a power interruption delay function in accordance with the present invention. In the display device of

Fig. 3, the voltage source V1 is connected to the input terminal of the H/V processor constant voltage circuit 131 through the power interruption delay charging circuit 370.

The power interruption delay charging circuit 370 includes a reverse voltage prevention diode D1 having its anode connected to the voltage source V1 and its cathode connected to the input terminal of the H/V processor constant voltage circuit 131, and a polarity capacitor C1 having its positive pole connected to a connection point of the cathode of the reverse voltage prevention diode D1 and the input terminal of the H/V processor constant voltage circuit 131 and its negative pole connected to the ground voltage terminal.

The operation of the display device with the above-mentioned construction in accordance with the present invention will hereinafter be described in detail.

When the display device is powered on, the high voltage from the high voltage source B+ is charged on the horizontal deflection coil H-DY and S-correction capacitor Cs through the field effect transistor FET1 and pulse transformer PT in the current amplifier 136 and then discharged through the discharge loop including the horizontal output transistor TR in the horizontal output circuit 134. Such charging and discharging operations are repeated as stated previously with reference to Fig. 2.

If the power supply to the display device is interrupted during the operation of the display device, the voltage supply to the H/V processor constant voltage circuit 131 is at once stopped in the display device of Fig. 2, as shown in Fig. 4a. However, according to the present invention, a voltage, charged on the polarity capacitor C1 during the power supply, is applied to the input terminal of the H/V processor constant voltage circuit 131, as shown in Fig. 4b, while it is discharged. As a result, the H/V processor constant voltage circuit 131 does not immediately stop the voltage supply to the H/V processor 132.

Noticeably, the reverse voltage prevention diode D1 is connected in series between the voltage source V1 and the H/V processor constant voltage circuit 131 to protect the power supply circuit by allowing the voltage charged on the polarity capacitor C1 not to be discharged to the voltage source V1 at the power interruption state.

Because the voltage charged on the polarity capacitor C1 is continuously applied to the H/V processor constant voltage circuit 131 until it is completely discharged, the voltage supply to the H/V processor 132 is not interrupted immediately. Therefore, the H/V processor 132 outputs the horizontal pulse signal continuously for a predetermined time period, as shown in Fig. 5b.

The continuous pulse output time of the H/V processor 132 is determined according to a discharge time of the polarity capacitor C1. As a result, the continuous pulse output time of the H/V processor 132 can be varied by adjusting the discharge time of the polarity capacitor C1.

While the output pulse from the H/V processor 132 maintains such a high voltage level as to continuously drive the field effect transistor FET2 in the horizontal driver 133, the horizontal drive transformer T2 continues to be excited to induce a voltage in its secondary coil, thereby causing the horizontal output transistor TR in the horizontal output circuit 134 to remain at its driven state. Hence, the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs can be sufficiently discharged. Namely, the discharge time of the high voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs is sufficient.

As apparent from the above description, according to the present invention, the power interruption delay charging circuit is provided at the input terminal of the H/V processor constant voltage circuit in the display device. The power interruption delay charging circuit can prevent the horizontal output transistor from being damaged due to an instantaneous surge current when power supply is resumed after power interruption. Further, the power interruption delay charging circuit

can prevent the peripheral devices and circuits from being successively damaged due to damage in the horizontal output transistor.

VI. ISSUES

Whether claims 1-11 are patentable under 35 U.S.C. §103(a) over Applicant's Admitted Prior Art (*hereafter*: AAPA) in view of Van Clifton Martin '348 (*hereafter:* Martin).

VII. GROUPING OF CLAIMS

Claim 1 stands or falls alone, and claims 2-11 stand or fall with claim 1.

VIII. ARGUMENT

Claims 1-11 are not obvious and unpatentable under 35 U.S.C. §103(a) in view of the combined teachings of the AAPA and Martin.

The rejection, is based on the Appellant's assessment of the prior art, and therefore, is reversible error.

A rejection under 35 USC §103 must be based on what was known prior to when the invention was made. The Appellant's assessment of the prior art, the problem confronted by the inventor, was not known to anyone prior to when the invention was made since there is no teaching of such an assessment except as set forth in the instant specification, and the instant specification was not known prior to when the invention was made.

An inventor's identification of a problem in the prior art can not be used as a evidence of motivation to modify the prior art. *In re Nomiya*, 184 U.S.P.Q. 607, at 612-13 (C.C.P.A. 1975). *In*

re Kaslow, 707 F.2d 1366, 1373, 217 USPQ 1089, 1094-95 (Fed. Cir. 1983) (quoting *In re Sponnoble*, 405 F.2d 578, 585, 160 USPQ 237, 243 (CCPA 1969)).

The Appellant's assessment of an "exemplary horizontal deflection circuit" suggests that the Appellant is of the opinion that the horizontal output circuit may by subject to damage when power supplied to a display device is interrupted.

> As the H/V processor operates no longer, it outputs no pulse signal thereby causing the high voltage charged on the horizontal deflection coil and S-correction capacitor not to be discharged. As a result, a voltage of about +120 to 160 V remains.
>
> Under the above condition, if the power supply to the display device is resumed, the H/V processor constant voltage circuit is driven because of application of a voltage so as to operate the H/V processor, a high voltage with a very high peak value (about +1.5 to 1.8KV) is instantaneously generated. As a result, a surge current resulting from the instantaneous high voltage abruptly flows through a discharge loop damaging a portion of the horizontal output circuit.
>
> If the horizontal output circuit is damaged, no horizontal deflection is performed on the screen of the display device, thereby causing a single line to be vertically drawn on the center of the screen. As a result, the user cannot recognize the information displayed on the screen.

Regarding claim 1, it has been held by a previous Board Decision, and relied on by the Examiner in the final rejection, that the AAPA teaches all that is claimed except the feature of*power interruption delay charging means for* ***gradually lowering said input voltage to said H/V processor constant voltage circuit*** *when power supplied to said display device is interrupted,* (emphasis added). The Appellant deems the that foregoing feature of claim 1 is non-obvious in view of the proposed combination of art.

The present invention provides a power interruption delay charging means for gradually lowering an input voltage to the H/V processor constant voltage circuit 131 when power supplied to a display device is interrupted in order to protect horizontal output circuit 134 consisting of

transistor TR.

Now, we must consider what Martin fairly teaches to one of ordinary skill in the art absent the teachings of the present application. Particular findings must be made as to the reason the skilled artisan, **with no knowledge of the claimed invention**, would have selected these components for combination in the manner claimed. *See In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317(Fed. Cir. 2000). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *See In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Martin's invention relates to a protection system for the screen of a cathode ray tube. Martin includes three protection control circuits 34, 35 and 36. In the final rejection and the Examiner's Answer the rejection did not apply any of the teachings in Martin regarding protection control circuits 34, 35 and 36, nor any of the teachings regarding how control circuit 36 relates to NPN transistor 56 and horizontal deflection yoke 17. Instead, the final rejection and the Examiner's Answer refer us to Martin's col. 2, lines 64-72, which state:

> The control grid 14 is clamped to a negative DC bias voltage -V1 from the power supply by a diode 44 connected between voltage -V1 and the control grid 14 and a capacitor 45 connected between the control grid 14 and ground. The output of the unblank driver 22 thereby controls the voltage between the control grid 14 and the cathode 13 by controlling the voltage of cathode 13. This diode-capacitor network makes the voltage at the control grid 14 drop slowly even though its bias voltage -V1 is removed.

Note here, however, that Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen.

Martin's teaching regarding protection control circuit 36 as it relates to NPN transistor 56 and horizontal deflection yoke 17 has been applied in the rejection.

Martin notes a problem that **a power loss could result in a high beam current and local overheating** of the screen, called phosphor or screen burn spots. See col. 1, lines 15-20. Accordingly, Martin **desires to prevent screen burn spots**, and **fails to teach** protection of a horizontal output circuit. There is no teaching in the applied art to suggest that damage to a horizontal output circuit will result in a high beam current and local overheating of the screen and cause screen burn spots.

Martin provides three parallel protection circuits (34, 35 and 36) **to prevent screen burn spots**: 1) protection circuit 34 is a cathode control circuit that will inhibit the beam current by controlling the voltage produced by unblank driver 22 for cathode 13; 2) protection circuit 35 is an accelerator grid control circuit that functions to short any voltage at accelerator grid 15 to ground; and 3) protection circuit 36 is a horizontal deflection control circuit that horizontally deflects the beam off the screen while the voltage at accelerator grid 15 is decaying to zero. According to Martin:

1) Cathode control circuit 34 includes an AND gate 42 that prevents beam generation when protection is required. Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen or any other protection function.

2) Accelerator grid control circuit 35 is necessary to short accelerator grid 15 to ground because the capacitance in capacitor 46 would normally prevent an immediate drop to zero.

3) Horizontal deflection control circuit 36 includes a transistor 58, resistors 61 and 62, relay coil 65, and relay contact 64. To prevent screen burn spots, transistor 58 is turned on

by the two bias voltages provided via resistors 61 or 62. These two bias voltages are arranged so that if one fails the other will be present. Also, the value of these bias voltages are chosen so that even if there is a power failure, **the voltages decay off at a slow enough rate so that transistor 58 will be turned on long enough** to cause the beam to be horizontally deflected off the screen, thereby preventing the beam from burning the screen.

In the rejection, we are referred to Martin's discussion of horizontal deflection yoke 17 and protection circuit 36, *i.e.*, horizontal deflection control circuit 36. In normal operation deflection of the beam by yoke 17 is controlled by X-yoke drive 101 over line 55 at the base of NPN transistor 56 which is connected between one side of the horizontal deflection yoke 17 and has a resistor 57 to ground..

Martin suggests that in order **to avoid damage to the screen** it is desired to cause the beam to be horizontally deflected off the screen. This is accomplished by protection circuit 36. In particular, a second NPN transistor 58 is normally off and is connected across transistor 56 with a current limiting resistor 59 connected therebetween. A positive DC bias voltage from the power supply +V3 is applied to the yoke 17. Transistor 58 is normally off and therefore current through transistor 56 controls the current through the horizontal deflection yoke 17 and thus the horizontal deflection of the beam. When it is necessary to protect the screen 16, the transistor 58 is turned on and additional current is drawn through the coil of the horizontal deflection yoke 17 so as to drive the beam off the screen.

According to the foregoing teaching found in Martin, one of ordinary skill in the art would have modified the AAPA to include a circuit similar to protection circuit 36 **in order to protect the screen** if it is shown that a similar problem would exist regarding the screen in the AAPA

Assuming, *arguendo*, that "causing a single line to be vertically drawn on the center of the screen" would damage the screen. Modifying the AAPA to prevent such a line is taught by Martin, that teaching being to drive the beam off the screen. **Accordingly, one of skill in the art would further look to Martin's protection circuit 36 which has the function of to driving the beam off the screen.**

Martin teaches that when the power supply fails, the horizontal deflection control circuit 36 provides protection by causing the voltage to transistor 58 to decay off at a slow enough rate to so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen.

Therefore, one of ordinary skill in the art not having a blueprint of the Appellant's invention as set forth in Appellant's claim 1, and having only Martin's teaching of horizontal deflection control circuit 36 which provides protection by causing a voltage to transistor 58 to decay off at a slow enough rate to so that transistor 58 will be turned on to cause the beam to be horizontally deflected off the screen, and seeking to modify AAPA would make such a modification by connecting a protection circuit 36, including transistor 58, to the AAPA's transistor TR of horizontal output circuit 134 in the same manner as taught by Martin.

Thus any voltage charged on the horizontal deflection coil H-DY and S-correction capacitor Cs will be discharged and the horizontal output circuit would not be damaged. Since there would be no damage to the horizontal output circuit, then horizontal deflection can be performed on the screen of the display device. Accordingly, there would be no cause for a single line to be vertically drawn on the center of the screen.

There is no suggestion in the applied art to look for a different solution to the problem taught

by Martin.

The Applicant does not find any reason not to rely on protection circuit 36 in applying Martin to the AAPA, the Applicant deems it to be reversible error, however, to apply Martin's protection circuit 36 in a manner not taught by Martin. To do so calls for an inventive solution.

"The statutory emphasis is on a person of *ordinary* skill. Inventors, as a class, according to the concept underlying the Constitution and the statutes that have created the patent system, possess something - call it what you will - which sets them apart from the workers of *ordinary* skill, and one should not go about determining obviousness under §103 by inquiring into what *patentees* (i.e., inventors) would have known or would have likely have done, faced with the revelations of references. A person of ordinary skill in the art is also presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate, whether by patient, and often expensive, systematic research or by extraordinary insights, it makes no difference which." See, *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448 at 454, 227 USPQ 293 at 297 (CAFC 1985).

In view of claim 1 of the present application, however, it is required that power interruption delay charging means be provided **for gradually lowering <u>an input voltage to the horizontal/vertical processor constant voltage circuit</u>** 131 of the AAPA when power supplied to the display device is interrupted.

In connecting protection circuit 36 to the AAPA's transistor TR of horizontal output circuit 134 in the same manner as taught by Martin, the input voltage to transistor 58 would decay off at a slow enough rate to so that transistor 58 will remain turned on long enough to cause the beam to be horizontally deflected off the screen, as desired and taught by Martin **to prevent screen burn**

spots on the screen. Note, that by modifying AAPA by connecting protection circuit 36 to the AAPA's transistor TR of horizontal output circuit 134 in the same manner as taught by Martin, **the result would be** that horizontal output circuit 134 and transistor TR in horizontal output circuit 134 would be protected.

Accordingly, if the modification of AAPA as taught by Martin results in the protection of AAPA's horizontal output circuit 134 and transistor TR, there would be no reason, and the applied art has not provided any other reason, to modify the AAPA to gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit.

Martin's teaching fails to suggest modification of the AAPA by **gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit** 131 of the AAPA, and the PTO has failed to provide a *prima facie* basis of support for suggesting that such a modification would have been obvious.

> *In re Rijckaert*, 28 USPQ2d 1955 (CAFC 1993) states:
>
> "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell,* 991 F.2d 781, 782, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) (quoting *In re Rhinehart,* 531 F.2d 1048, 1051, 189 USPQ 143, 147 (CCPA 1976). If the examiner [Board] fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988).

Thus far, it has been shown that taking into account only what is taught by the prior art, **there is no teaching** which would have fairly suggested to one of ordinary skill in the art any reason to provide power interruption delay charging means for gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit 131 of the AAPA when power supplied to the display device is interrupted.

Accordingly, the rejection of claim 1 is deemed to be in error and should not be sustained.

Looking to the Board's decision in Paper No. 25, we have attempted to ascertain why the Board (not the applied art) suggested that providing power interruption delay charging means for gradually lowering an input voltage to the horizontal/vertical processor constant voltage circuit 131 of the AAPA when power supplied to the display device is interrupted would have been obvious.

It appears that the Board's statement on page 9, lines 13-17 of paper No. 25, *i.e.*, "we find Martin's additional teaching of slowly decaying the voltage to the horizontal deflection yoke would have suggested to an artisan gradually dropping the voltage of the voltage source V1 of the horizontal/vertical constant voltage circuit [131] of the [AAPA]" to be key to the Board's finding.

Looking again to Martin, we find no such teaching of "slowly decaying the voltage to the horizontal deflection yoke." Martin teaches slowly decaying the voltage to the control grid 14. Martin also teaches that the voltage applied to transistor 58 in the protection circuit 36 also slowly decays. However, Martin's voltage -V1 to the horizontal deflection yoke 17 is **not** slowly decayed, nor is the slowly decaying voltage of the protection circuit 36 in Martin provided to the deflection yoke 17. The slowly decaying voltage of the protection circuit 36 in Martin goes no further than the base of transistor 58, turning transistor 58 on long enough to draw extra current through deflection yoke 17 in order to drive the beam off the screen **to prevent screen burn spots** on the screen.

Accordingly, there is **no** *prima facie* showing that an artisan would have been taught to provide the slow voltage decay circuit of the horizontal deflection control circuit 36 of Martin at the voltage source V1 of the horizontal/vertical constant voltage circuit 131 of the AAPA instead of at transistor TR in the same manner it is connected to Martin's transistor 56.

In Paper No. 27, page 6, lines 16-20, however, the Board finds that the artisan would have provided the slow voltage decay circuit of the horizontal deflection control circuit 36 of Martin at the voltage source V1 of the horizontal/vertical constant voltage circuit 131 of the AAPA, instead of at transistor TR in the same manner it is connected to Martin's transistor 56, "because that is where the supply voltage is located, and because the current would flow to transistor TR, via circuits 131-133."

The Board fails to take into account, however, that Martin only teaches decaying the input voltage to protection circuit 36, and that by modifying AAPA to include the protection circuit 36 by connecting protection circuit 36 to the base of transistor TR (AAPA), then a new input voltage would exist, that being the input voltage applied to the base of transistor 58 (Martin). It is this input voltage that Martin desires to slowly decay in order to protect the screen by allowing the beam to deflect off the screen. Martin does not teach slowly decaying an input voltage to any other synchronization circuit.

Accordingly, the rejection of claim 1 is deemed to be in error and should not be sustained.

In Paper No. 27, page 6, lines 20+, the Board held, "[i]n addition, because Martin discloses that the protection circuits are provided to regulate the input circuits to inhibit high beam current which would otherwise damage the screen, an artisan would be taught to provide the horizontal deflection control circuit 36 to the H/V processor constant voltage circuit 131."

The Board's use of the phrase "regulate the input circuits" is overly broad, because Martin only teaches regulating voltages applied to various components of the cathode ray tube. There are **no** "input circuits" (see Fig. 2) being regulated in Martin, there are only **certain outputs** of the circuits shown in Fig. 2 being regulated .

As noted previously, Martin notes a problem that a power loss could result in a **high beam current** and local overheating of the screen, called phosphor or screen burn spots. See col. 1, lines 15-20. Martin provides three parallel protection circuits (34, 35 and 36) to prevent screen burn spots: 1) protection circuit 34 is a cathode control circuit that will inhibit the beam current **by controlling the voltage produced** by unblank driver 22 for cathode 13; 2) protection circuit 35 is an accelerator grid control circuit that functions **to short any voltage at accelerator grid 15 to ground**; and 3) protection circuit 36 is a horizontal deflection control circuit that **horizontally deflects the beam off the screen while the voltage at accelerator grid 15 is decaying to zero**.

1) Cathode control circuit 34 includes an AND gate 42 that prevents beam generation when protection is required. Martin **does not** teach that diode 44 and cathode 45 function to **protect** the screen or any other protection function.

2) Accelerator grid control circuit 35 is necessary to short accelerator grid 15 to ground because the capacitance in capacitor 46 would normally prevent an immediate drop to zero.

3) Horizontal deflection control circuit 36 includes a transistor 58, resistors 61 and 62, relay coil 65, and relay contact 64. To prevent screen burn spots, transistor 58 is turned on by the two bias voltages provided via resistors 61 or 62. These two bias voltages are arranged so that if one fails the other will be present. Also, the value of these bias voltages are chosen so that even if there is a power failure, the voltages decay off at a slow enough rate so that transistor 58 will be turned on long enough to cause the beam to be horizontally deflected off the screen, thereby preventing the beam from burning the screen.

Martin clearly does not suggest regulating any "input circuits," there are only **certain outputs** of the circuits shown in Fig. 2 being regulated.

Accordingly, the rejection of claim 1 is deemed to be in error and should not be sustained.

IX. CONCLUSION

The Appellant has shown that the rejection relies on the Appellant's assessment of the prior art, and not on what was taught by the teachings of the prior art itself. An inventor's identification of a problem in the prior art can not be used as a evidence of motivation to modify the prior art. *In re Nomiya*, supra.

The Appellant has shown that, absent any knowledge of the Appellant's invention/claims, one of ordinary skill in the art would not have been motivated by the teachings of the applied art, to provide a power interruption delay charging means for gradually lowering an input voltage to a H/V processor constant voltage circuit when power supplied to a display device is interrupted is not taught by the prior art.

The Appellant has shown that one of ordinary skill in the art would have been taught by Martin's desire to protect a display screen to modify the AAPA by providing a protection circuit to cause a beam current to be horizontally deflected off a screen in the same manner as disclosed in Martin in order to protect the screen, not to protect a horizontal output circuit, nor any other circuit.

The Appellant has shown that modifying the AAPA in a manner not taught by Martin would require innovation instead of ordinary skill in the art. A person of ordinary skill in the art is presumed to be one who thinks along the line of conventional wisdom in the art and is not one who undertakes to innovate, whether by patient, and often expensive, systematic research or by extraordinary insights, it makes no difference which." See, *Standard Oil Co. v. American Cyanamid Co.*, supra.

The Appellant has shown that any other interpretation of Martin, other than that agreed to

by the Appellant, is erroneous, and thus is deemed to be reversible error.

Accordingly, it has been shown that the applied art fails to teach all that is claimed and that claim 1 is non-obvious and patentable over the applied art for the reasons stated above. As such, claims 2-11 are deemed non-obvious and patentable over the applied art for the same reasons as claim 1.

Respectfully submitted,

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X. APPENDIX

CLAIMS UNDER APPEAL

1. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a current amplifier for amplifying current in response to the pulse width modulation signal from said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

2. The display device as set forth in claim 1, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

3. A display device with a power interruption delay function, comprising:

a power supply circuit for converting a received commercial AC power into a DC input voltage;

a horizontal deflection circuit under the control of a microcomputer, receiving said DC input voltage, for horizontally deflecting electron beams generated in said display device; and

power interruption delay charging means for gradually lowering said DC input voltage received by said horizontal deflection circuit when said AC power supplied to said power supply circuit is interrupted, said power interruption delay charging means comprising:

a polarity capacitor for performing a charging operation when said AC power is supplied and a discharging operation when said AC power is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to said power supply circuit when said AC power is interrupted.

4. The display device as set forth in claim 3, wherein said horizontal deflection circuit comprises:

a pulse width modulation controller for generating a pulse width modulation signal under the control of said microcomputer;

a current amplifier for amplifying current in response to said pulse width modulation signal generated by said pulse width modulation controller;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

a horizontal deflection coil for horizontally deflecting said electron beams;

a S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver; and

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to said DC input voltage, said DC input voltage being received through said power interruption delay charging means.

5. The display device as set forth in claim 4, wherein said current amplifier comprises:

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor FET1 having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to said ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source B+ and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal.

6. The display device as set forth in claim 5, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

7. The display device as set forth in claim 6, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a

drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.

8. A display device with a power interruption delay function, comprising:

a pulse width modulation controller for generating a pulse width modulation signal under the control of a microcomputer;

a horizontal deflection coil for horizontally deflecting electron beams generated in said display device;

a current amplification transformer having a primary coil and a secondary coil;

a field effect transistor having its gate terminal connected to one terminal of said secondary coil;

one terminal of said primary coil being connected to an output terminal of said pulse width modulation controller through a capacitor and another terminal of said primary coil being connected to a ground terminal;

said field effect transistor having a drain terminal connected to a high voltage source and a source terminal connected in common to a second terminal of said secondary coil and one side of a pulse transformer;

said pulse transformer having a second side connected to one side of said horizontal

deflection coil;

a first diode connected between said source terminal and said drain terminal; and

a second diode connected between said second terminal of said secondary coil and said ground terminal;

a H/V processor for generating a square wave pulse signal under the control of said microcomputer;

a horizontal driver for generating a drive pulse signal in response to the square wave pulse signal from said H/V processor;

an S-correction capacitor connected in series between said horizontal deflection coil and a ground terminal, for correcting a linearity of center-to-left and right sides of a screen;

a horizontal output circuit for charging and discharging energy on said horizontal deflection coil and said S-correction capacitor in response to an output signal from said current amplifier and said drive pulse signal from said horizontal driver;

a H/V processor constant voltage circuit for supplying a constant voltage to said H/V processor in response to an input voltage; and

power interruption delay charging means for gradually lowering said input voltage to said H/V processor constant voltage circuit when power supplied to said display device is interrupted.

9. The display device as set forth in claim 8, wherein said power interruption delay charging means includes:

a polarity capacitor for performing a charging operation when power is supplied to said display device and a discharging operation when the power supplied to said display device is interrupted; and

a diode connected to said polarity capacitor, for preventing a voltage charged on said polarity capacitor from being discharged to a power supply circuit when the power supplied to the display device is interrupted.

10. The display device as set forth in claim 8, wherein said horizontal output circuit comprises a horizontal output transistor having a collector terminal connected in common to said second side of said pulse transformer and said one side of said horizontal deflection coil, an emitter terminal connected to said S-correction capacitor and said ground terminal, and a base terminal connected to an output terminal of said horizontal driver for receiving said drive pulse signal.

11. The display device as set forth in claim 10, wherein said horizontal driver comprises:

a second field effect transistor having a gate terminal connected to receive said square wave pulse signal from said H/V processor, a source terminal connected to said ground terminal, and a drain terminal;

a horizontal drive transformer having a primary coil and a secondary coil, said primary coil having one terminal connected to a voltage source through a resistor and a second terminal connected to said drain terminal of said second field effect transistor; and

said secondary coil of said horizontal drive transformer having one side connected to said base terminal of said horizontal output transistor and a second side connected to said ground terminal.